

FAIRCHILD DIGITAL

CMOS

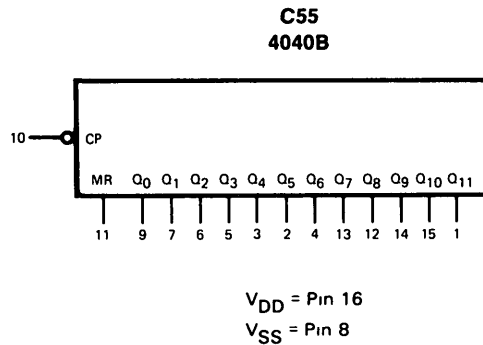
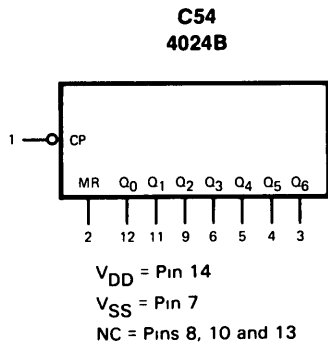
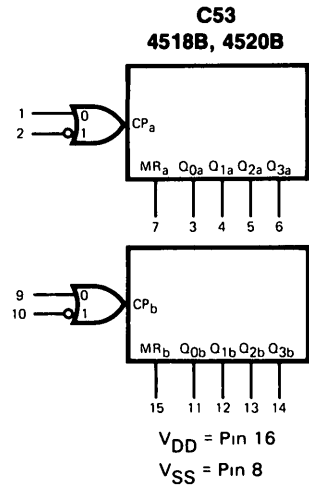
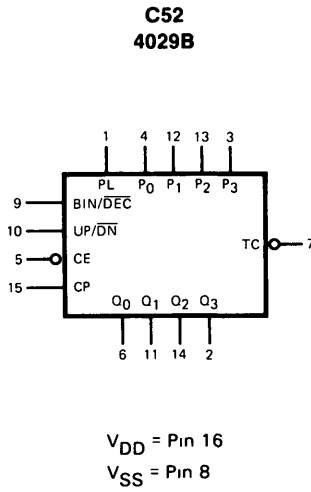
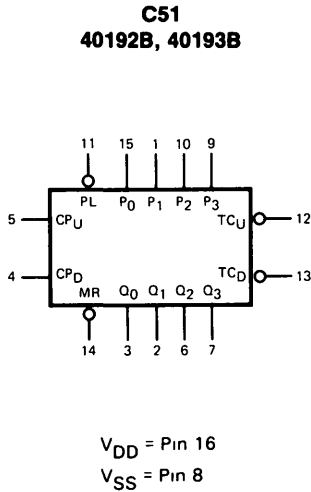
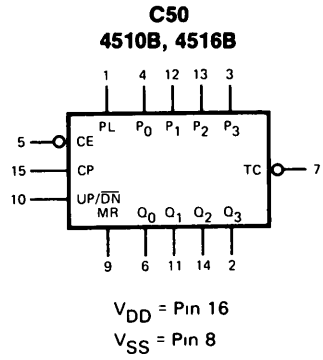
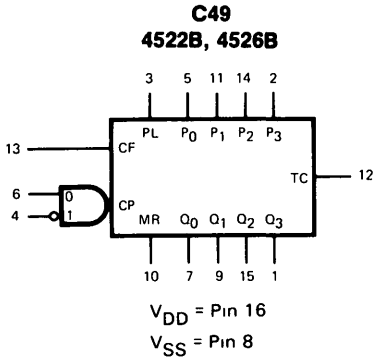
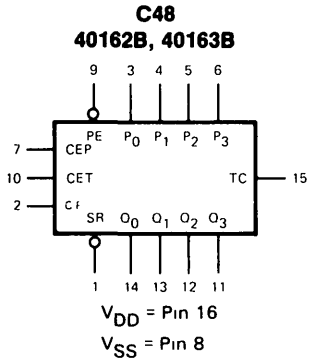
COUNTERS (Cont'd)

Item	Function	DEVICE NO.	Modulo	Parallel Load ⁽¹⁾	Clock Transition	Max Clock Rate MHz (Typ) VDD = 10V	Clock to Q Output Delay ns (Typ) VDD = 10V	Logic/Connection Diagram	Package(s)
1	4-Bit Sync Count Up/Down	40193B	Binary	A	L→H	8 0	105	C51	4L,6B,9B
2	4-Bit Sync Count Up/Down	4029B	Decade or Binary	A	L→H	12	62	C52	4L,6B,9B
3	Dual 4-Bit Sync Count Up	4518B	Decade	—	L→H or H→L	10	95	C53	4L,6B,9B
4	Dual 4-Bit Synchronous Count Up	4520B	Binary	—	L→H or H→L	10	95	C53	4L,6B,9B
5	7-Bit Ripple Count Up	4024B	Binary	—	H→L	30	45	C54	3I,6A,9A
6	12-Bit Ripple Count Up	4040B	Binary	—	H→L	25	55	C55	4L,6B,9B
7	14-Bit Ripple Count Up	4020B	Binary	—	H→L	25	55	C56	4L,6B,9B
8	4-Bit Johnson Counter	4022B ⁽²⁾	1-of-8	—	L→H or H→L	16	95	C57	4L,6B,9B
9	5-Bit Johnson Counter	4017B	1-of-10	—	L→H or H→L	13 8	114	C58	4L,6B,9B
10	5-Bit Johnson Counter	4018B ⁽²⁾	—	—	L→H	10	115	C59	4L,6B,9B
11	Bit Rate Generator	4702B	14-Bit Rates	—	L→H	6 5	40	C60	4L,6B,9B
12	21-Stage Binary Counter	4045B	Binary	—	L→H	25	900	C89	3I,6A,9A
13	24-Stage Binary Counter	4521B	Binary	—	H→L	12	3200	C90	4L,6B,9B
14	Real Time 5-Decade Counter	4534B	Decade (x5)	—	L→H	4 5	1000	C91	4M,6N,9N
15	3-Digit BCD Counter	4553B	Decade (x3)	—	L→H or H→L	6 0	300	C92	4L,6B,9B
16	7-Stage Counter	4727B	Binary	—	L→H	8 0	90	C93	3I,6A,9A
17	7-Stage Counter	4737B	Binary	—	L→H	8 0	90	C95	3I,6A,9A
18	Programmable Timer/Counter	4722B	Binary	—	H→L	6 0	1000	C94	4L,6B,9B
19	Industrial Time Base Generator	4566B	Decade	—	H→L	3 2	400	C99	4L,6B,9B

1 A = Asynchronous S = Synchronous
2 To be announced

FAIRCHILD LOGIC/CONNECTION DIAGRAMS

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NOTE The Flatpak versions have the same pinouts (Connection Diagram) as the Dual In-Line Packages